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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/569,942	02/28/2006	Akihiko Endo	P29123	1077

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EXAMINER	
NIKMANESH, SEAHVOSH J	
ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
08/07/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com
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Office Action Summary	Application No.	Applicant(s)	
	10/569,942	ENDO ET AL.	
	Examiner	Art Unit	
	SEAHVOSH J. NIKMANESH	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/7/2008 and 2/8/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to the IDS filed 2/8/2008.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statements filed 2/8/2008 and 6/7/2006 have been considered.

4. Please note that the foreign patent documents listed on the 6/7/2006 IDS have been considered, but were added to the PTO 892 to correct the citation numbers and copies of which have already been filed by the applicant.

Drawings

5. Figures 3 and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Henley et al., US 6,146,979.

a. **Regarding claim 1,** Henley et al. shows a method for manufacturing a bonded wafer, comprising the steps of:

ion-implanting of a light element into a wafer (10) for active layer at a predetermined depth via an insulating film (19) that has been formed thereon to form an ion-implanted area in said active layer wafer;

subsequently bonding said active layer wafer with a supporting wafer (52) having an insulating film formed thereon (54) together as their insulating films facing to each other to produce the bonded wafer (Fig.6); and

heat treating said bonded wafer to form bubbles (11) of said light element in said ion-implanted area and thereby induce a cleavage and separation of a part of said bonded wafer (15) defined in said ion-implanted side for forming an active layer (Figs.4-7; Column 4, line 39 through Column 6, line 43).

8. Claim 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Cheung et al., US 6,344,404 B1.

a. **Regarding claim 1,** Cheung et al. shows a method for manufacturing a bonded wafer, comprising the steps of:

ion-implanting of a light element (2109; Column 4, lines 48-51) into a wafer (2100; Column 4, line 35) for active layer (2101; Column 4, line 36) at a predetermined depth via an insulating film (2102; Column 4; line 41-43) that has been formed thereon to form an ion-implanted area (2111; Column 4, line51-52) in said active layer wafer;

subsequently bonding said active layer wafer with a supporting wafer (2201) having an insulating film (2203; Column 5, lines 31-59) formed thereon together as their insulating films (2305) facing to each other to produce the bonded wafer; and

heat treating said bonded wafer to form bubbles of said light element in said ion-implanted area and thereby induce a cleavage and separation of a part of said bonded wafer defined in said ion-implanted side for forming an active layer (Figs. 2-7; Column 4, line 27-Column 6, line 66).

b. **Regarding claim 3,** Cheung et al. shows a method for manufacturing a bonded wafer in which said active layer wafer and said supporting wafer are subjected to a plasma treatment, respectively, before said bonding step of said active layer wafer with said supporting wafer (Column 5, lines 54-64).

9. Claim 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Linn et al., US 6,255,195 B1.

a. **Regarding claim 1,** Linn et al. shows a method for manufacturing a bonded wafer, comprising the steps of:

ion-implanting (23) of a light element into a wafer for active layer (25) at a predetermined depth via an insulating film (21) that has been formed thereon to form an ion-implanted area in said active layer wafer;

subsequently bonding said active layer wafer with a supporting wafer (11) having an insulating film formed thereon together as their insulating films facing to each other to produce the bonded wafer (Column 5, lines 28-45); and

heat treating said bonded wafer to form bubbles of said light element in said ion-implanted area and thereby induce a cleavage and separation of a part of said bonded wafer defined in said ion-implanted side for forming an active layer (Figs. 2A-3; Column 4, lines 30-46; Column 5, lines 9-45).

b. **Regarding claim 2,** Linn et al. discloses that the thickness of the oxide insulator is 1-50 nm and the thickness of the formed semiconductor layer is 0.1-2μm (Column 4, lines 1-16). The specified range given by Linn et al. allows for the applicants formula to be satisfied

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung et al., US 6,344,404 B1.

a. **Regarding claim 4,** Cheung shows that plasma treatment is carried out in an atmosphere of oxygen gas or nitrogen gas by holding said wafers at a temperature of 400 °C or lower

Cheung et al. does not show that the wafers are treated for ten seconds or longer.

However, it would have been obvious to one of ordinary skill in the art at the time the invention as made to have treated the semiconductor for over 10 seconds since plasma treatments require time to generate and sufficient time is needed for plasma to interact with the semiconductor materials. The examiner notes that no time window is explicitly stated by Cheung, however the specified gases of oxygen are disclosed for the purpose of plasma cleaning of the substrate surface (Column 5, lines 54-60) and the process would require sufficient time to activate the wafer surface. Also Cheung et al. discloses that when working with the ion implanted region it is crucial to keep the substrate processing temperatures between 20°C and 450°C in order to maintain bubble formation at the ion implanted region (Column 5, lines 15-30) prior to the wafer bonding and separation processes.

12. Claims 2, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung et al., US 6,344,404 B1 further in view of Linn et al., US 6,255,195 B1.

a. **Regarding claim 2,** Cheung et al. shows the invention substantially as claimed pertaining to claim 1 above and that the insulation layer (2102) is relatively thin compared to the active region (2101;Fig. 2).

Cheung et al. does not show that the thickness of said insulating film of said active layer wafer, tdox, satisfies the following formula:
tdox < (1/9) X tsoi, where tsoi = thickness of said active layer.

Linn et al. teaches that the thickness of the oxide insulator is 1-50 nm and the thickness of the formed semiconductor layer is 0.1-2μm (Column 4, lines 1-16). The specified range given by Linn et al. allows for the applicants formula to be satisfied.

It would have been obvious to one of ordinary skill in the art the time the invention was made to have utilized the specified thicknesses as disclosed in Linn et al. with the method of Cheung et al. to utilize process conditions which satisfy applicants claimed range since Linn et al. discloses that the thickness of the oxide insulator is 1-50 nm and the thickness of the formed semiconductor layer is 0.1-2μm (Column 4, lines 1-16). The combined teachings allows for the applicants formula to be satisfied at any point wherein the oxide is kept to a minimum in comparison to the formed semiconductor layer which would be done

so with the motivation that maintaining a minimally thick insulating oxide layer allows for the proper adhesion properties while keeping undulation of the silicon surface to a minimum, thus allowing for improved bonding and material characteristics in regards to wafer bonding utilizing implantation techniques. The combination can be met with a reasonable expectation for success since the teachings are related to the use of insulation layers to improve adhesion between bonded wafers in order to for active layers.

b. Regarding claim 5, Cheung et al. shows a method for manufacturing a bonded wafer in which said active layer wafer and said supporting wafer are subjected to a plasma treatment, respectively, before said bonding step of said active layer wafer with said supporting wafer (Column 5, lines 54-64).

c. **Regarding claim 6,** Cheung shows that plasma treatment is carried out in an atmosphere of oxygen gas or nitrogen gas by holding said wafers at a temperature of 400 °C or lower

Cheung et al. does not show that the wafers are treated for ten seconds or longer.

However, it would have been obvious to one of ordinary skill in the art at the time the invention as made to have treated the semiconductor for over 10 seconds since plasma treatments require time to generate and sufficient time is needed for plasma to interact with the semiconductor materials. The examiner notes that no time window is explicitly stated by Cheung, however the specified

gases of oxygen are disclosed for the purpose of plasma cleaning of the substrate surface (Column 5, lines 54-60) and the process would require sufficient time to activate the wafer surface. Also Cheung et al. discloses that when working with the ion implanted region it is crucial to keep the substrate processing temperatures between 20°C and 450°C in order to maintain bubble formation at the ion implanted region (Column 5, lines 15-30) prior to the wafer bonding and separation processes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEAHVOSH J. NIKMANESH whose telephone number is (571)270-1805. The examiner can normally be reached on Mon through Fri 7:30 - 5:00 E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Seahvosh J Nikmanesh/
Examiner, Art Unit 2812

/Scott B. Geyer/
Primary Examiner, Art Unit 2812